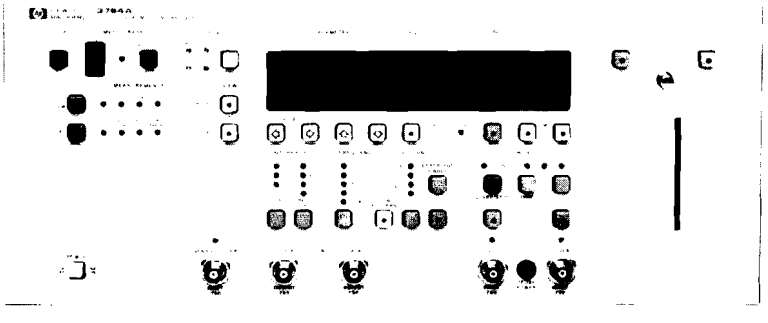
HP 3764A

DIGITAL TRANSMISSION ANALYZER



HEWLETT PACKARD

HP 3764A: Error Measurement at 139 Mb/s

Except where otherwise indicated, the following parameters are warranted performance specifications. Parameters described as "typical" or "nominal" are supplemental characteristics which provide a useful indication of typical, but non-warranted, performance characteristics.

Generator

Internal Clock

Frequency: 139.264 MHz.
Setting Tolerance: ± 1 ppm.
Temperature Stability:
0 to +35°C: ± 3 ppm.
-10 to +55°C: ± 10 ppm.
Aging: Typically < ± 5 ppm per year.
Fixed Frequency Offsets:
In accordance with CCITT Rec G.703 at 139M.
+ΔF: 139.264 MHz + 15 ppm (139.266 MHz).
-ΔF: 139.264 MHz - 15 ppm (139.262 MHz).

External Clock Input

Frequency: 1 kHz to 170 MHz.
Triggering: Nominal ground. Nominal ECL or TTL thresholds selectable by internal link.
Amplitude: 300 mV to 3V pk-pk within ± 3V dc max.
Impedance: Nominal 75Ω to ground (or to -2V selectable by internal link).
Protection: 125 mA fuse.

Clock Monitor Output
(Rear Panel)

Format: Allows access to the unjittered transmitter clock (whether internal or external).
Amplitude: Nominal ECL levels.
Impedance: Low, unbalanced to ground.
External Load: 75Ω to -2V, dc coupled, 75Ω to ground, ac coupled.
Protection: 125 mA fuse.

Patterns

PRBS: 2^{23}-1 is automatically set in accordance with CCITT Rec O.151. 2^{15}-1 may be manually selected. Polynomial for PRBS 23 is $D^{23} + \overline{D^{18}} + 1 = 0$ (inverted sequence). Longest run of zeros is 23.
Polynomial for PRBS 15 is $D^{15} + \overline{D^{14}} + 1 = 0$ (inverted sequence). Longest run of zeros is 15.
Word: Variable length from 1 to 16 bits.
Alternating Word: External signal controls output of two words; changeover is synchronous with the end of a word. The words can be varied in length from 1 bit to 8 bits.
AIS: Continuous "all ones" pattern.

Alternating Word Control Input (Rear Panel)

Trigger Level: Nominally ground.
Amplitude: 5V rms max.
Sensitivity: 250 mV pk-pk square wave dc to 100 kHz; 500 mV pk-pk sine triangular wave 200 Hz to 100 kHz.
Impedance: Nominal 1kΩ unbalanced to ground.

Error Add - Binary Errors

Rate: Average error ratio of 1 error in 1000 clock periods (1 x 10^{-3}).
Single: One error introduced for each press of the Single Error Add key.

Pattern Trigger Output
(Rear Panel)

Format: One pulse per PRBS or Word pattern.
Width: Nominally two clock periods.
Amplitude: 1V pk-pk min.
Impedance: Nominal 50Ω unbalanced.
Protection: Open/short circuit protected.

Coded Data Output

Bit Rate: 139.264 Mb/s.
Format: Coded Mark Inversion (CMI).
Amplitude: ± 0.5V ± 10%.
Impedance: Nominal 75Ω, unbalanced to ground.
Return Loss: > 15 dB, 7 MHz to 210 MHz.
Pulse Shape: Conforms to CCITT Rec G.703.
Protection: Open/short circuit protected.

Binary Data Output

Format: RZ or NRZ.
Bit Rate:
RZ: 1 kb/s to 150 Mb/s.
NRZ: 1 kb/s to 170 Mb/s.
Amplitude: Nominal ECL levels.
Impedance: Nominal 75Ω unbalanced to -2V.
RZ Duty Cycle: Nominally 50 ± 10% on internal clock.
NRZ Width: 100% ± 5%.
Transition Times: < 1.8 ns.
Total Edge Jitter: 0.5% of period + 350 ps.
Overshoot/Preshoot: < 10% pulse amplitude.

Clock Output

Duty Cycle (when using internal clock): 50 ± 10%.
Amplitude: Nominal ECL levels.
Impedance: 75Ω unbalanced.
External Load: 75Ω to -2V dc coupled; 75Ω to ground ac coupled.
Intrinsic Jitter: < 0.5% period +50 ps pk-pk (eg. at 1 kHz, < 0.005 UI pk-pk; at 170 MHz, < 0.0135 UI pk-pk).
Protection: 125 mA fuse.

Receiver

Coded Data Input

Bit Rate: 139M ± 3 Mb/s.
Format: Coded Mark Inversion (CMI).
Amplitude: Nominal max pk-pk voltage into 75Ω is 1V.
Jitter Tolerance:
Better than 10 UI pk-pk up to 100 kHz.
Better than 0.5 UI pk-pk at 2 MHz.
Equalization: Automatic equalization conforming to CCITT Rec G.703 for cable loss of up to 12 dB at half bit rate.
Monitor Mode: An additional gain of 26 dB is available to allow for flat loss at equipment monitor points.
Impedance: Nominal 75Ω unbalanced to ground.
Return Loss: > 15 dB, 7 MHz to 210 MHz.
Polarity: Data or $\overline{\text{Data}}$ switched at the binary level.
Protection: 125 mA fuse.

Binary Data Input

Format: RZ or NRZ.
Bit Rate:
RZ: 1 kb/s to 150 Mb/s.
NRZ: 1 kb/s to 170 Mb/s.
Amplitude: Nominal ECL levels.
Impedance: Nominal 75Ω unbalanced to -2V.
Polarity: Data or $\overline{\text{Data}}$ switched at the binary level.
Protection: 125 mA fuse.

Binary Clock Input

Rate: 1 kHz to 170 MHz.
Amplitude: Nominal ECL levels.
Impedance: Nominal 75Ω unbalanced to -2V.
Polarity: Clock or $\overline{\text{Clock}}$.
Protection: 125 mA fuse.

External Error Mode

Format: 1 pulse per error, minimum pulse width 3 ns, input to the Data Input port. Parameters otherwise the same as for the Binary Data Input.
Clock: An external clock must be supplied, parameters are the same as for the Binary Clock Input.

Receiver Clock Monitor Output (Rear Panel)

Source: Recovered Clock or Binary Clock Input.
Amplitude: Nominal ECL levels.
Impedance: Unbalanced, low.
External Load: 50Ω to -2V dc coupled, or 50Ω to ground ac coupled.
Protection: 125 mA fuse.

Synchronization - Automatic

Automatic for rates above 500 kb/s only.
Sync Loss: Greater than 10,000 errors in 90,000 clock periods.
Sync Gain: Less than 10 errors in 90 clock periods.

Synchronization - Manual

Operation: Pressing the Manual Sync key will initiate a resynchronization.

External Sync Input (Rear Panel)

Format: A logic "0" to "1" transition on this input initiates a resynchronization when Ext Sync Control is selected.
Amplitude: Nominal ECL levels.
Impedance: Nominal 50Ω unbalanced to -2V.
Pulse Width: Minimum 20 ns.
Protection: 125 mA fuse.

Receiver Pattern Trigger Output (Rear Panel)

Format: One pulse per PRBS or Word pattern.
Width: Nominally two clock periods.
Amplitude: 1V pk minimum.
Impedance: Nominal 50Ω unbalanced to ground.
Protection: Open/short circuit protected, max voltage ± 5V short term.

Error Output (Rear Panel)

Format: One edge per error. When a data loss is detected the error output port will give a continuous stream of errors. When a Sync Loss is detected the output port will give an output equivalent to every alternate bit in error.
Amplitude: Minimum 1V pk-pk about ground.
Impedance: Nominal 50Ω to ground, unbalanced.
Protection: Open/short circuit protected, max voltage ± 5V short term.

Auxiliary Inputs

The status of the auxiliary inputs may be selected for front panel display or printing on the printer. If printing is selected, a printout occurs if there is a change of state on any of the seven digital inputs, or if the voltage on the one analog input passes through the printing threshold.

Auxiliary Input - Digital

Format: 3 inputs are nominal ECL levels, impedance 50Ω to -2V; the other 4 are nominal TTL levels.
Protection: 125 mA fuse.

Auxiliary Input - Analog

Format: Voltage range -12.7 to +12.7V.
Resolution: 100 mV.
Impedance: Nominal 1MΩ to ground.
Protection: 125 mA fuse.
Printing Threshold: May be set in the range -12.7V to +12.7V in steps of 0.1V. The threshold has a ± 0.2V hysteresis. Default value 5.0V.

Measurement Timing

Real-time Clock

Function: Provides time and date information for event logging, gating period timing, and error performance measurements.
Date: Shows day, month, year. The clock allows for leap years.
Local Time: shows hours, minutes and seconds.
Elapsed Time: Shows time since the start of a gating period in days, hours, minutes and seconds.
Source: Internal crystal oscillator with battery back-up. Greater than 6 months operation without recharge (automatic when instrument connected to power supply).
Accuracy: Typically ± 1/3 second per day at 20°C.

Gating Period

Manual: Gating Start/Stop key is used to control the length of the gating period.
Single: Started by pressing the Gating Start/Stop key and terminated at the end of the gating period.
Repeat: Started by pressing Gating Start/Stop key. When one period ends, a new one starts until the measurement is terminated by pressing the Gating Start/Stop key again. There is no "dead time" between gating periods.
Min Gating Period: 1 second.
Max Gating Period: 99 days, 23 hours, 59 minutes, 59 seconds.
Resolution: 1 second.

Measurement Results Display

During Manual or Single gating periods the display shows the accumulating results. During repetitive gating periods the display can show either the results obtained at the end of the previous gating period or the accumulating results for the current gating period. In the event of clock signal loss when measuring in binary mode, the message "CL" is displayed.

Error Measurements

The receiver detects bit errors by comparing the incoming data bit-by-bit with the internally generated reference pattern. Error measurements can be made on bit errors detected internally, or on errors detected by external equipment. In the latter case, a signal is input to the Data Input in the form of one pulse per error.

Error Ratio

The ratio of counted errors to the number of clocks in the selected gating period. The result is displayed in the form X.Y x 10^{-N} where N is in the range 1 to 15. If the result is based on < 100 errors the display is truncated to X x 10^{-N}.

Error Count

The number of errors is counted over the selected gating period. The result is displayed in individual counts up to 99,999 then in the form X.Y x 10^{N}, where N is an integer in the range 5 to 15.

Error Seconds

The number of seconds in the gating period which contain at least one error. The result is displayed as for Error Count.

Error Free Seconds

The number of seconds in the gating period which contain no errors. The result is displayed as for Error Count.

Error Analysis

% Unavailability

The error ratio is calculated over consecutive 1 second timed intervals during the gating period. An unavailable period starts when the error ratio is greater than a preset threshold for at least 10 consecutive 1 second intervals. These 10 seconds are assumed part of the unavailable time. The unavailable period ends when the error ratio is less than the preset threshold for 10 consecutive second. These 10 seconds are assumed part of the available time. % Unavail is the percentage of seconds in the overall gating period which are deemed unavailable.
Threshold: Can be set in the range 10^{-1} to 10^{-6}. Default value 10^{-3}.

% Severely Errored Seconds

Severely errored seconds are those 1 second intervals in the available time with an error ratio worse than a preset threshold. The available time is obtained by subtracting the unavailable time from the gating period. % SES is the percentage of seconds in the available time which exceed the threshold.
Threshold: Can be set in the range 10^{-1} to 10^{-6}. Default value 10^{-3}.

% Degraded Minutes

The number of severely errored seconds is subtracted from the total available time and the remaining seconds are regrouped into packets of 60. Degraded minutes are those packets for which the error ratio is greater than a preset threshold. % DM is the percentage of packets which exceed this threshold.
Threshold: Can be set in the range 10^{-3} to 10^{-9}. Default value 10^{-6}.

% Error Seconds

The ratio of the number of errored seconds to the total number of available seconds in the gating period, expressed as a percentage. During periods of system unavailability, the measurement counters freeze.

Flags

Current system conditions such as data pattern synchronization loss (SL), data loss (DL), alarm indication signal received (AI) and unavailability (UA) are displayed in the order of occurrence on the Flags display.

Flags are latched by the instrument to provide a record of events during the measurement period in order of occurrence. These may be viewed on the Parameter display.

If a loss of power occurs while the instrument is in use, the message "Power Loss" will be shown in the Parameter display.

HP-IB Interface

Modes: Addressable or Talk Only.
Flags: Remote, Listen, Talk and SRQ are indicated by LED.
Implementation: IEEE Std 488 - 1978 implementation is as follows: SH1; AH1; T5; TE0; L4; LE0; SR1; RL1; PP0; DC1; DT0; C0; E1.

The HP-IB capability conforms to IEEE Std 728-1982 for Codes and Formats.

Result Logging

The HP 3764A is fitted with an internal, 20-column printer. The HP-IB port may be used in "Talk-only" mode to print results on an external 80-column wide format device such as the HP ThinkJet printer.

Internal Printer

Printing Speed: Typically 0.7 lines per second.
Buffer Store: Approximately 270 lines.
Print Formatting Modes:
On Demand: Prints time and status of selected parameters when key is pressed.
Printer On: Prints a user selected set of parameters on one of the following conditions:
(1) Always at the end of the gating period.
(2) Only when the error count exceeds zero errors in a gating period.
(3) Only when the error ratio exceeds 1 x 10^{-N} where N can be set to an integer in the range 1 to 15.

In addition the following can be selected:
Error Hit Seconds: Time of occurrence and number of errors in each errored second is printed.
Auxiliary Inputs: Status of the auxiliary inputs is printed.

External Printer

Format: 80-column, all 8 parameters printed on one line.
Buffer Store: Approximately 70 lines.

General

Power Supply: 190 to 253V or 90 to 126V ac, 48 Hz to 66 Hz.
Power Consumption: Not more than 400 VA.
Probe Power: HP active probes may be powered from the HP 3764A's connector. Supplies available: +15V, -12.6V and ground.

Physical

Dimensions: 178 mm high; 425 mm wide; 440 mm deep (7.0 in x 16.7 in x 17.3 in).
Net Weight: 15 kg (33 lb) approximately, depending on option.
Shipping Weight (inc front panel cover): 27 kg (59 lb).

Environmental

Operating Temperature Range: 0 to 50°C.
Storage Temperature Range: -40 to 75°C.

Option 001: Error Measurement at 2, 8 and 34 Mb/s

All the specifications for HP 3764A with Option 001 are the same as for the standard instrument, except for those listed below.

Generator

Internal Clock

Frequency: 2.048 (2M), 8.448 (8M), 34.368 (34M), and 139.264 (139M) MHz.
Setting Tolerance: ± 1 ppm.
Temperature Stability:
0 to +35°C: ± 3 ppm.
-10 to +55°C: ± 10 ppm.
Aging: Typically < ± 5 ppm per year.
Fixed Frequency Offsets: These are available as a separate option. See the specification for Option 005 on page 17 for more information.

External Clock Input

Mounted on the rear panel when Option 005 fitted.
Parameters: As for the External Clock Input of the standard instrument.

Patterns

PRBS: Automatically set to suit bit rate in accordance with CCITT Rec O.151: 2^{15}-1 when data rate is set to 2 and 8M; 2^{23}-1 when data rate is set to 34 and 139M. The PRBS polynomials are the same as for the standard instrument.
Word: As standard instrument.
Alternating Word: As Standard instrument.
AIS: As Standard instrument.

Coded Data Output

Bit Rate: 2, 8, 34 and 139M.
Format:
2, 8 and 34M: HDB3.
139M: CMI.
Amplitude:
2 and 8M: Nominal 2.37V pk.
34M: Nominal 1.0V pk.
139M: Nominal 0.5V pk.
Impedance: Nominal 75Ω unbalanced to ground.
Return Loss at 139M: >15 dB, 7 to 210 MHz.
Pulse Shape: Typically conforms to CCITT Rec G.703.
Protection: Open/short circuit protected, max voltage ± 5V short term.

Binary Data Output

Bit Rate: Internal fixed rates or using an external clock as follows:
When Frequency Position 2, 8 or 34M is selected: 1 kb/s to 50 Mb/s.
When Frequency Position 139M is selected: 1 kb/s to 150 Mb/s RZ; 1 kb/s to 170 Mb/s NRZ.
Format: RZ or NRZ.
Amplitude:
Frequency Position 2, 8 and 34M: Nominal TTL levels.
Frequency Position 139M: Nominal ECL levels.
Impedance:
TTL: Nominal 75Ω to ground.
ECL: Nominal 75Ω to -2V.
Protection: 125 mA fuse.

Clock Output

Bit Rate: As selected for Coded or Binary Data.
Amplitude:
Frequency Position 2, 8 and 34M: Nominal TTL levels.
Frequency Position 139M: Nominal ECL levels.
Impedance:
TTL: Nominal 75Ω to ground.
ECL: Nominal to -2V.
Protection: 125 mA fuse.

Receiver

Coded Data Input

Bit Rate: 2, 8, 34 and 139M.
Rate Tolerance: ± 1%.
Format:
2, 8 and 34M: HDB3.
139M: CMI.
Amplitude:
2 and 8M: Nominal 2.37V pk.
34M: Nominal 1.0V pk.
139M: Nominal 0.5V pk.
Jitter Tolerance: Better than CCITT Rec G.823.
Equalization: Automatic equalization for cable loss. Compensation for max loss at 2 and 8M is 6 dB, and at 34 and 139M is 12 dB.
Monitor Mode: Provides additional flat gain for operation at protected monitor points. This gain is 30 dB at 2 and 8M, and 26 dB at 34 and 139M.
Impedance:
2, 8 and 34M: Nominal 75Ω to ground.
139M: Nominal 75Ω to -2V.
Return Loss at 139M: >15 dB, 7 to 210 MHz.
Polarity: Data or $\overline{\text{Data}}$, switched at the binary level.
Protection: 125 mA fuse.

Binary Data Input

Bit Rate:
When Frequency Position 2, 8 or 34M is selected: 1 kb/s to 50 Mb/s.
When Frequency Position 139M is selected: 1 kb/s to 150 Mb/s RZ; 1 kb/s to 170 Mb/s NRZ.
Amplitude:
2, 8 and 34M: Nominal TTL levels.
139M: Nominal ECL levels.
Impedance:
2, 8 and 34M: Nominal 75Ω to ground.
139M: Nominal 75Ω to -2V.
Protection: 125 mA fuse.

Binary Clock Input

Rate:
When Frequency Position 2, 8 and 34M is selected: 1 kHz to 50 MHz.
When Frequency Position 139M is selected: 1 kHz to 170 MHz.
Amplitude:
2, 8 and 34M: Nominal TTL levels.
139M: Nominal ECL levels.
Impedance:
2, 8 and 34M: Nominal 75Ω unbalanced to ground.
139M: Nominal 75Ω unbalanced to -2V.
Polarity: Clock or $\overline{\text{Clock}}$.
Protection: 125 mA fuse.

Option 002: Jitter at 139 Mb/s

All the specifications for HP 3764A with Option 002 are the same as for the standard instrument, except for those listed below.

Generator

Internal Jitter Modulation

Fixed Jitter Frequency Points:

100 Hz	1 kHz	10 kHz	100 kHz	1 MHz
200 Hz	2 kHz	20 kHz	200 kHz	2 MHz
500 Hz	5 kHz	50 kHz	500 kHz	3.5 MHz
				4 MHz

Frequency/Amplitude:

Frequency Range	Amplitude (UI pk-pk)
100 Hz to 5 kHz	0 to 10.0
10 kHz to 2 MHz	0 to 1.00
At 3.5 MHz	0 to 0.75
At 4 MHz	0 to 0.50

Amplitude Steps:
100 Hz to 5 kHz: 0.1 UI pk-pk.
10 kHz to 4 MHz: 0.01 UI pk-pk.
Frequency Accuracy: Crystal controlled, better than 0.1%.
Absolute Accuracy: (Referred to Generator Clock Monitor Output and measured on the 0 to 1 transition of the clock output)

Frequency Range	Amplitude Accuracy
100 Hz to 5 kHz	As for Ext Jitter Mod, range 10
10 kHz to 4 MHz	As for Ext Jitter Mod, range 1

Intrinsic Jitter:
5 kHz and below: ≤ 0.2 UI pk-pk.
10 kHz and above: ≤ 0.01 UI pk-pk.

External Jitter Modulation

The following specifications are for a sinusoidal modulating signal.
Range:

	Frequency Range	Amplitude (UI pk-pk)
Range 1	2 Hz to 2 MHz	0 to 1.15
	2 MHz to 3.5 MHz	0 to 0.75
	3.5 MHz to 5 MHz	0 to 0.50
Range 10	2 Hz to 100 kHz	0 to 11.5

Max Input Voltage: 10V pk-pk.
Nominal Sensitivity:
Range 1: 5V/UI pk-pk at 1 kHz;
Range 10: 0.5V/UI pk-pk at 1 kHz.
Absolute Accuracy of Indicated Amplitude:
(Referred to Generator Clock Monitor Output and measured on the 0 to 1 transition of the clock output)
Range 1: better than ± 3% ± 0.01 UI pk-pk to 1 MHz; additional degradation >1 MHz less than ± 5%.
Range 10: better than ± 3% ± 0.1 UI pk-pk.
Intrinsic Jitter:
Range 10: ≤ 0.02 UI pk-pk.
Range 1: ≤ 0.01 UI pk-pk.
Impedance: Nominal 50Ω unbalanced to ground.

Receiver

Jitter can be measured either on a clock recovered from the CMI coded input data or on the binary input clock.
Reference Clock: This is derived internally from the input data/clock or can be supplied externally to the Jitter Reference Clock Input.

Jitter Reference Clock Input
(Rear Panel)

Frequency Range: External jitter reference must be within ± 20 ppm of 139.264 MHz.
Note: This input clock should be phase coherent with the data signal.
Amplitude: Nominal ECL levels.
Impedance: Nominal 75Ω to ground, unbalanced.

Demodulated Jitter Output
(Rear Panel)

Amplitude Scaling:
Range 1: 5.0V/UI pk-pk;
Range 10: 0.5V/UI pk-pk.
Impedance: Nominal voltage source, minimum load nominally 50Ω to ground.
Accuracy: As per measurement circuit (when terminated 50Ω to ground).
Bandwidth: Nominally 2 Hz to 3.5 MHz.

Jitter Measurement Input
(Rear Panel)

Impedance: Nominal 50Ω to ground.
Sensitivity:
Range 1: 0.2 UI/V pk-pk;
Range 10: 2.0 UI/V pk-pk.

Jitter Measurement Gating Period

Manual: Gating Start/Stop key is used to control the length of the gating period.
Single: Started by pressing the Gating Start/Stop key and terminated at the end of the gating period.
Repeat: Started by pressing Gating Start/Stop key. When one period ends, a new one starts until the measurement is terminated by pressing the Gating Start/Stop key again.
Min Gating Period: 1 second.
Max Gating Period: 99 days, 23 hours, 59 minutes, 59 seconds.
Resolution: 1 second.

Jitter Measurement

All jitter measurements are made over a selected gating period.

Jitter Amplitude

Max value of pk-pk timing jitter in the gating period.

	Jitter Amplitude Range*	
	1 UI	**10 UI**
Max jitter amplitude (UI pk-pk)	1.15	11.5
Lowest specified freq		
(Internal Reference)	200 Hz	200 Hz
(External Reference)	Nominally 2 Hz	Nominally 2 Hz
Highest specified freq	3.5 MHz	10 kHz

*** Covers CCITT Rec O.171, Table 3.**

Range 1

Accuracy (at 1 kHz):
Internal Reference: ± 3%
± 0.01 UI pk-pk.
External Reference: ± 3%
± 0.02 UI pk-pk.

Intrinsic Jitter: Typically ≤ 0.01 UI pk-pk (as measured on binary clock with HP1 filter and internal reference frequency).

Range 10

Accuracy (at 1 kHz):
Internal Reference: ± 3% ± 0.1 UI pk-pk.
External Reference: ± 3% ± 0.2 UI pk-pk.
Intrinsic Jitter: Typically ≤ 0.1 UI pk-pk (as measured on binary clock with HP1 filter and internal reference frequency).
Additional Degradation Factors: Applicable to ranges 1 and 10.
Frequency Response:
< 200 Hz: Less than ± 5%.
100 kHz to 1 MHz: Less than ± 2%.
1 MHz to 3.5 MHz: Less than ± 5%.
Pattern Dependency: Typically ≤ 0.05 UI pk-pk (CMI; 2^{23}-1 PRBS; LP and HP1 filters).

Jitter Hit Count

The number of times in the jitter gating period that the received jitter amplitude exceeds a user-set threshold.
Threshold Range:
Range 1: 0 to 1.00 UI pk-pk in steps of 0.01 UI.
Range 10: 0 to 10.0 UI pk-pk in steps of 0.1 UI.
Display: The result is displayed in individual counts up to 99,999 then in the form X.Y x 10^N, where N is an integer in the range 5 to 15.
Sensitivity: Typically > 30 ns width to count.

Jitter Hit Seconds

The number of seconds in which at least one jitter hit occurred. The result is displayed as for Error Count.

Jitter Hit Free Seconds

The number of seconds in which no jitter hits occurred. The result is displayed as for Error Count.

Error/Hit Output

(Rear Panel)

Format: One edge per event. This is a dual purpose port. The output indicates the receipt of either an error or a jitter hit depending on the selected measurement. See standard instrument specifications

Internal Filters

Bandlimit the demodulated jitter signal before jitter amplitude measurement and before providing a demodulated jitter output on the rear panel.
The three internal filters are as specified in CCITT Rec O.171.

Filter	Type	Nominal 3 dB Corner Frequency	Nominal Slope Asymptote
HP1	High Pass	200 Hz	20 dB/decade
HP2	High Pass	10 kHz	20 dB/decade
LP	Low Pass	3.5 MHz	60 dB/decade

It is possible to select these filters as follows:
Off (measurement circuit is connected directly to the jitter demodulator); LP; HP1; HP2; LP + HP1; LP + HP2; Ext (to allow connection of external filter between the Demodulated Jitter Output port and the Jitter Measurement Input port).

Option 003: Additional Data Outputs at 139 Mb/s

All specifications for the HP 3764A with Option 003 are as for the standard instrument, except for those listed below.

This option provides three data outputs on the rear panel in addition to the main data output on the front panel.

Data Outputs

Format: CMI or binary RZ or NRZ.
Bit Rate:
CMI: 139.264 Mb/s.
RZ or NRZ: 1 kb/s to 140 Mb/s.
Delays:
Main Data Output to Delayed Data Output 1: Approximately half the 2^{23}-1 PRBS length. These are in phase when word patterns are selected.
Delayed O/P 1 to Delayed O/P 2: ≥ 1 bit.
Delayed O/P 2 to Delayed O/P 3: ≥ 1 bit.
Other parameters are as for standard instrument.

External Clock Input

Frequency: 1 kHz to 140 MHz.
Other parameters are as for standard instrument.

Option 005: Fixed Frequency Offsets

Can only be ordered with Option 001.

This option allows fixed clock frequency offsets to be selected in accordance with CCITT Rec G.703 at 2, 8, 34 and 139M.

Center Frequency (MHz)	Offset (ppm)	-ΔF (MHz)	+ΔF (MHz)
139.264	± 15	139.262	139.266
34.368	± 20	34.3673	34.3687
8.448	± 30	8.44775	8.44825
2.048	± 50	2.04790	2.04810

A front panel LED indicates when either a frequency offset or the External Clock Input is selected.

Other specifications are as for the Internal Clock in standard unit generator.

For variable frequency offsets up to ± 100 ppm, see Option 006.

Option 006: Multirate Error Measurement + Clock Synthesizer

All the specifications for HP 3764A with Option 006 are the same as for the standard instrument, except for those listed below.

Generator

Internal Clock

Fixed Rates: 0.704 (0.7M), 2.048 (2M), 8.448 (8M), 34.368 (34M), 139.264 (139M) MHz.
Variable Rates: 1 kHz to 170 MHz with 6-digit resolution.
Initial Setting Error: < ± 1 ppm.
Stability: < ± 2 ppm over temperature range 0 to 55°C.
Aging: < ± 2 ppm per year.

A front panel LED indicates when the synthesizer clock rate is within 4 ppm of the indicated rate. (Typically within 3 seconds and to within 1 ppm approximately 2 seconds later.)

External Clock Input

Frequency Range: 1 kHz to 170 MHz.
Triggering: Nominal ground, ECL, TTL, Variable or Automatic thresholds selectable from front panel.
Amplitude: 300 mV to 5V pk-pk within ± 5V dc max.
Impedance: Nominal 75Ω to ground or -2V selectable from front panel.
External Clock Frequency Measurement Resolution:
1.00 kHz to 999.999 kHz: ± 2 Hz.
1.00 MHz to 170 MHz: 6 digits.
Accuracy: As internal clock plus additional error < ± 2 ppm.
Protection: 125 mA fuse.

Frequency Offsets

Fixed: In accordance with CCITT Rec. G.703. 0.7M ± 50 ppm; 2M ± 50 ppm; 8M ± 30 ppm; 34M ± 20 ppm; 139M ± 15 ppm.
Variable: Up to ± 100 ppm.
Resolution: 1 ppm.

Patterns

PRBS: Automatically set in accordance with CCITT Rec O.151. 2^{15}-1 when data rate of 0.7, 2 or 8M is selected. 2^{23}-1 when data rate of 34 or 139M is selected. PRBS can be selected manually if required. The PRBS polynomials are as for the standard instrument.
Word: As standard instrument.
Alternating Word: As standard instrument.
AIS: As standard instrument.

Coded Data Output

Bit Rate: 0.7, 2, 8, 34 and 139M.
Offsets: Fixed and variable.
Format:
0.7, 2, 8 and 34M: HDB3.
139M: CMI.
Amplitude:
0.7, 2, 8M: Nominal 2.37V pk.
34M: Nominal 1.00V pk.
139M: As standard instrument.
Impedance: Nominal 75Ω unbalanced to ground.
Return Loss at 139M: > 15 dB, 7 to 210 MHz.
Pulse Shape: Conforms to CCITT Rec G.703.
Protection: Open/short circuit protected.

Binary Data Output

Bit Rate:
Fixed: 0.7, 2, 8, 34 and 139M.
Variable and External: 1 kb/s to 170 Mb/s.
Offsets: Fixed and variable.
Format: RZ or NRZ.
Amplitude:
0.7, 2, 8 and 34M: Nominal TTL.
139M: Nominal ECL.
1 kb/s to 50 Mb/s: Nominal TTL or ECL selectable.
50 Mb/s to 170 Mb/s: Nominal ECL.
Impedance:
TTL: Nominal 75Ω unbalanced to ground.
ECL: Nominal 75Ω unbalanced to -2V.
Transition Times:
TTL: < 5 ns.
ECL: < 2 ns.
Protection: 125 mA fuse.

Clock Output

Rate: As Coded or Binary Data.
Duty Cycle: 50 ± 10% for internal clock.
Amplitude:
0.7, 2, 8 and 34M: Nominal TTL.
139M: Nominal ECL.
1 kb/s to 50 Mb/s: Nominal TTL or ECL selectable.
50 Mb/s to 170 Mb/s: ECL.
Note: Selection of TTL or ECL is common for both Binary Data and Clock.
External Load:
TTL: 75Ω.
ECL: Either 75Ω to -2V dc coupled, or 75Ω to ground ac coupled.
Protection: 125 mA fuse.

Receiver

Coded Data Input

Bit Rate: 0.7, 2, 8, 34 and 139M.
Bit Rate Tolerance: ± 1%.
Format:
0.7, 2, 8 and 34M: HDB3.
139M: CMI.
Amplitude:
0.7, 2, 8 and 34M: Nominal 2.37V pk.
139M: Nominal 1.00V pk.
Equalization: Conforms to CCITT Rec G.703.
Monitor Mode: At each input rate there is a "Monitor Mode" which provides additional flat gain for operation at protected monitor points:
0.7, 2 and 8M: 30 dB.
34 and 139M: 26 dB.
Impedance:
0.7, 2, 8 and 34M: Nominal 75Ω unbalanced to ground.
139M: Nominal 75Ω unbalanced to -2V.
Return Loss at 139M: > 15 dB, 7 to 210 MHz.
Polarity: Data or $\overline{\text{Data}}$ switched at the binary level.
Protection: 125 mA fuse.

Binary Data Input

Bit Rate: 1 kb/s to 170 Mb/s.
Format: RZ or NRZ.
Amplitude:
0.7, 2, 8 and 34M: Nominal TTL levels.
139M: Nominal ECL level.
1 kb/s to 50 Mb/s: Nominal TTL or ECL selectable.
50 Mb/s to 170 Mb/s: ECL.
Impedance:
TTL: Nominal 75Ω unbalanced to ground.
ECL: Nominal 75Ω unbalanced to -2V.
Polarity: Data or $\overline{\text{Data}}$ switched at the binary level.
Protection: 125 mA fuse.

Binary Clock Input

Rate: 1 kHz to 170 MHz.
Amplitude: As Binary Data Input.
Impedance: As Binary Data Input.
Polarity: Clock or $\overline{\text{Clock}}$.
Protection: 125 mA fuse.

Option 007: Jitter at 139 Mb/s, Through-data + Clock Synthesizer

All the specifications for HP 3764A with Option 007 are as for the standard instrument except for those listed below.

Generator

Internal Clock

Fixed Rates: 0.704 (0.7M), 2.048 (2M), 8.448 (8M), 34.368 (34M), 139.264 (139M) MHz.
Variable Rates: 1 kHz to 170 MHz with 6-digit resolution.
Initial Setting Error: < ± 1 ppm.
Stability: < ± 2 ppm over temperature range 0 to 55°C.
Aging: < ± 2 ppm per year.

A front panel LED indicates when the synthesizer clock rate is within 4 ppm of the indicated rate. (Typically within 3 seconds and to within 1 ppm approximately 2 seconds later.)

External Clock Input

Frequency Range: 1 kHz to 170 MHz.
Triggering: Nominal ground, ECL, TTL, Variable or Automatic thresholds selectable.
Amplitude: 300 mV to 5V pk-pk within ± 5V dc max.
Impedance: Nominal 75Ω to ground or -2V selectable.
External Clock Frequency Measurement Resolution:
1.00 kHz to 999.999 kHz: ± 2 Hz.
1.00 MHz to 170 MHz: 6 digits.
Accuracy: As internal clock plus additional error < ± 2 ppm.
Protection: 125 mA fuse.

Patterns

PRBS: Automatically set in accordance with CCITT Rec O.151: 2^{15}-1 when data rate 0.7, 2 or 8M is selected. 2^{23}-1 when data rate 34 or 139M is selected. PRBS can be selected manually if required. The PRBS polynomials are as for the standard instrument.
Word: As standard instrument.
Alternating Word: As standard instrument.
AIS: As standard instrument.

Coded Data Output

Bit Rate: 139M.
Offsets:
Fixed: ± 15 ppm.
Variable: Up to ± 100 ppm in 1 ppm steps.
Format: CMI.
Amplitude: As Standard instrument, ± 0.5V ± 10%.
Impedance: Nominal 75Ω unbalanced to ground.
Return Loss: > 15 dB, 7 to 210 MHz.
Pulse Shape: Conforms to CCITT Rec G.703.
Protection: Open/short circuit protected.

Binary Data Output

Bit Rate:
Fixed: 0.7, 2, 8, 34 and 139M.
Variable and External: 1 kb/s to 170 Mb/s.
Offsets:
Fixed: 0.7M ± 50 ppm; 2M ± 50 ppm; 8M ± 30 ppm; 34M ± 20 ppm; 139 ± 15 ppm.
Variable: Up to ± 100 ppm in 1 ppm steps.
Format: RZ or NRZ.
Amplitude: Nominal ECL levels.
Impedance: Nominal 75Ω unbalanced to -2V.
Transition Time: < 2 ns.
Protection: 125 mA fuse.

Clock Output

Rate: As Coded or Binary Data.
Duty Cycle: 50 ± 10% for internal clock.
Amplitude: Nominal ECL levels.
External Load: Either 75Ω to -2V dc coupled or 75Ω to ground, ac coupled.
Protection: 125 mA fuse.

Jitter Modulation

Jitter can be added to any internally generated PRBS or Word pattern or to a signal applied in the Through-data mode.

The specifications for the jitter generation and measurement are as described in Option 002.

Through-Data

Allows jitter to be added to any nominally jitter-free 139.264 Mb/s CMI or binary ECL signal applied to the receiver. If binary data is applied, a corresponding clock signal must be supplied to the Through-Data Clock Input. The output signal is CMI encoded.

Through-Data Input - Coded

Bit Rate: 139M ± 100 ppm.
Format: CMI.
CMI data is decoded before jitter is added and then encoded again, so polarity of encoded 1s is not necessarily preserved.
Amplitude: Nominal max pk-pk voltage into 75Ω is 1V.
Equalization: Automatic equalization conforming to CCITT Rec G.703 for cable loss of up to 12 dB at half bit rate.
Impedance: Nominal 75Ω unbalanced to ground.
Protection: 125 mA fuse.

Through-Data Input - Binary Data and Clock

Bit Rate: 139M ± 100 ppm.
Data Format: NRZ recommended.
Amplitude: Nominal ECL levels.
Impedance: Nominal 75Ω to -2V.
Protection: 125 mA.

Through-Data Output

Bit Rate: Same as Input Data.
Format: CMI.
Amplitude: ± 0.5V ± 10%.
Impedance: Nominal 75Ω unbalanced to ground.
Pulse Shape: Conforms to CCITT Rec G.703.
Protection: Open/short circuit protected, max voltage ± 5V short term.

General

Power Consumption: Not more than 450 VA.
Operating Temperature Range: 0 to 45°C.

Option 010: Tape Cartridge Unit

Cannot be ordered with Option 007.

This option replaces the internal printer with a tape cartridge unit for data logging of results and storage of measurement presets.
Storage Capacity of Tape: Approx 210K characters.
Storage Format: 80 characters per "line".
Buffer Store: Approximately 70 lines.

Environment

Operating Temperature Range: 0 to 35°C.
Storage Temperature Range: -40°C to +75°C.

Modes

Results Store: Measurement results, system messages, time and date information may be recorded on tape.
Results Recall: The data stored on the tape may be read by two methods:

(a) Directly in a personal computer. The tape format is compatible with the HP 85 and the cartridge may be read in this machine using a suitable program.
(b) Indirectly via a data transfer through the HP-IB port. HP-IB compatible devices will be able to input this data.

Settings Store: The contents of the measurement preset NVM may be stored on the tape via this control.
Settings Recall: The contents of the measurement preset NVM may be recalled from the tape via this control.

Instruments Covered By Manual

Attached to the rear panel of the instrument is a serial number plate. The serial number plate has a four digit serial prefix, a reference letter denoting country of origin (U = United Kingdom) and a five digit serial number. The serial prefix is the same for all identical instruments, it changes only when a change is made to the instrument. The serial number is unique to each instrument and should be quoted in all correspondence with Hewlett-Packard, especially when ordering replacement parts.

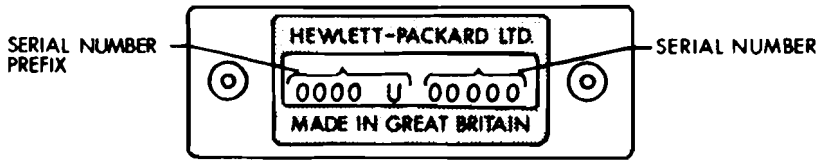


Figure 1-1. Serial Number Plate

Options

The Options available in the HP 3764A Digital Transmission Analyzer allow the instrument to be configured to fit a wide range of applications. The Options available are :-

Option 001	Provides Pattern generation; Error measurement & analysis at the four main CEPT rates of 2.048 Mbit/s, 8.448 Mbit/s, 34.368 Mbit/s & 139.264 Mbit/s.
Option 002	Provides Pattern generation; Error measurement & analysis: Jitter generation & measurement at 139.264 Mbit/s.
Option 003	Provides three additional Data Outputs which are delayed with respect to the main Data output.
Option 006	Provides Pattern generation; Error measurement & analysis at the five main CEPT rates of 704 kbit/s, 2.048 Mbit/s, 8.448 Mbit/s, 34.368 Mbit/s & 139.264 Mbit/s. The Frequency synthesizer also provides two variable frequency rates from 1 kbit/s to 170 Mbit/s and a selection of fixed and variable frequency Offsets for all available rates.
Option 007	Provides Pattern generation; Error measurement & analysis at 139.264 Mbit/s. The frequency synthesizer also provides two variable frequency rates from 1 kHz to 170 MHz and a selection of fixed and variable frequency Offsets. Jitter generation & measurement is provided at 139.264 MHz only. In addition a THRU Data capability is provided which allows Jitter to be added to, 139.264 Mbit/s CMI Coded Data or 139.264 MHz Binary clock. This Option excludes the Tape Cartridge option (010), and the internal Printer .
Option 010	The internal printer is replaced by a Tape Cartridge Unit. This Option is not possible in conjunction with Option 007.
Option 907	Front Handle Kit.

Option 908	Rack Flange Kit.
Option 909	Rack & Handle Kit.
Option 910	Provides a double set of Operating & Service manuals & an Extender card.
Option 915	Provides a Service manual & an Extender card.

Accessories

The following accessories are supplied with the HP 3764A digital Transmission Analyzer :-

Protective Front Panel Cover

Power Cable

Spare Roll of Printer Paper (See Note)

Note

If Option 010 (Tape Cartridge Unit) is ordered the spare roll of printer paper is replaced by a Tape Cartridge.

If Option 007 (THRU Data) is ordered neither the spare roll of printer paper nor a Tape Cartridge is provided.

The following accessory is available for use with the HP 3764A Digital Transmission Analyzer and can be purchased through your nearest Hewlett-Packard Sales & Service office.

HP 15508B 75Ω Unbalanced/110 Ω Balanced Converter.