JEDEC STANDARD NO. 22-A110 TEST METHOD A110 HIGHLY-ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST (HAST)

1.0 PURPOSE

The Highly-Accelerated Temperature and Humidity Stress Test is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It employs severe conditions of temperature, humidity, and bias which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. The stress usually activates the same failure mechanisms as the "85/85" Steady-State Humidity Life Test (JEDEC Standard No. 22-A101).

2.0 APPARATUS

The test requires a pressure chamber capable of maintaining a specified temperature and relative humidity continuously, while providing electrical connections to the devices under test in a specified biasing configuration.

2.1 The chamber must be capable of providing controlled conditions of pressure, temperature and relative humidity during ramp-up to, and ramp-down from, the specified test conditions. Calibration records shall verify that the equipment avoids condensation on devices under test (DUTs) hotter than 50°C during ramp-up and ramp-down for conditions of maximum thermal mass loading and minimum (zero) DUT power dissipation. Calibration records shall verify that, for steady state conditions and maximum thermal mass loading, test conditions are maintained within the tolerances specified in Sec. 3.1.

2.2 A permanent record of the temperature profile for each test cycle is recommended, so that the validity of the stress can be verified.

2.3 Devices under stress must be distributed to minimize temperature gradients. Devices under stress shall be no closer than 3 cm from internal chamber surfaces, and must not be subjected to direct radiant heat from heaters. Boards on which devices are mounted should be oriented to minimize interference with vapor circulation.

2.4 Care must be exercised in the choice of board and socket materials, to minimize release of contamination, and to minimize degradation due to corrosion and other mechanisms.

2.5 Ionic contamination of the test apparatus (card cage, test boards, sockets, wiring, storage containers, etc.) shall be controlled to avoid test artifacts.

2.6 De-ionized water with a minimum resistivity of 1 megaohm-cm at room temperature shall be used.

3.0 TEST CONDITIONS

Test conditions consist of a temperature, relative humidity, and duration used in conjunction with an electrical bias configuration specific to the device.

3.1 **Temperature, Relative Humidity and Duration.**

Temperature (dry bulb °C)[1]	Relative Humidity(%)[1]	Temperature (wet bulb, °C)[2]	Vapor Pressure (psia) [2]	Duration (hours)[3]
130 ± 2	85 ± 5	124.7	33.5	96 (-0,+2)

Notes:

1. Tolerances apply to the entire useable test area.
2. For information only.
3. The test conditions are to be applied continuously except during any interim readouts. Note: For interim readouts, devices should be returned to stress within the time specified in Sec. 4.5.
4. For parts that reach absorption equilibrium in 24 hours or less, 96 hours at 130°C/85% RH is equivalent to at least 1000 hours at 85°C/85% RH. For parts that require more than 24 hours to reach equilibrium at 130°C/85% RH, the time should be extended appropriately.
5. Caution: For plastic-encapsulated microcircuits, it is known that moisture reduces the effective glass transition temperature of the molding compound. Stress temperatures above the effective glass transition temperature may lead to failure mechanisms unrelated to standard 85/85 stress.

3.2 **Biasing Guidelines**

3.2.1 Apply bias according to the following guidelines:

3.2.1.1 Minimize power dissipation.

3.2.1.2 Alternate pin bias as much as possible.

3.2.1.3 Distribute potential differences across chip metallization as much as possible.

3.2.1.4 Maximize voltage within operating range.

3.2.2 Either of two kinds of bias can be used to satisfy these guidelines, whichever is more severe:

3.2.2.1 *Continuous bias.* The dc bias shall be applied continuously. Continuous bias is more severe than cycled bias when the die temperature is ≤ 10°C higher than the chamber ambient temperature. or, if the die temperature is not known, when the heat dissipation of the DUT is less than 200mW. If the heat dissipation of the DUT exceeds 200mW, then the die temperature should be calculated. If the die temperature

exceeds the chamber ambient temperature by more than 5°C then the die temperature rise above the chamber ambient should be included in reports of test results since acceleration of failure mechanisms will be affected.

3.2.2.2 *Cycled bias.* The dc voltage applied to the devices under test shall be periodically interrupted with an appropriate frequency and duty cycle. If the biasing configuration results in a temperature rise above the chamber ambient, ΔT_{ja}, exceeding 10°C, then cycled bias, when optimized for a specific device type, will be more severe than continuous bias. Heating as a result of power dissipation tends to drive moisture away from the die and thereby hinders moisture-related failure mechanisms. Cycled bias permits moisture collection on the die during the off periods when device power dissipation does not occur. Cycling the DUT bias with a 50% duty cycle is optimal for most plastic-encapsulated microcircuits. The period of the cycled stress should be ≤ 2 hours for packages ≥ 2 mm in thickness and ≤ 30 minutes for packages < 2 mm in thickness. The die temperature, as calculated on the basis of the known thermal impedance and dissipation, should be quoted with the results whenever it exceeds the chamber ambient by 5°C or more.

Criteria for choosing continuous or cyclical bias, and whether or not to report the amount by which the die temperature exceeds the chamber ambient temperature, are summarized in the table:

ΔT_{ja}	**Cyclical Bias?**	**Report ΔT_{ja}?**
ΔT_{ja} < 5°C, or Power per DUT < 200mW	No	No
(ΔT_{ja} ≥ 5°C or Power per DUT ≥ 200mW), and ΔT_{ja} < 10°C	No	Yes
ΔT_{ja} ≥ 10°C	Yes	Yes

4.0 PROCEDURE

The test devices shall be mounted in a manner which exposes them to a specified condition of temperature and humidity with a specified electrical biasing condition. Exposure of devices to excessively hot, dry ambients or conditions which result in condensation on devices and electrical fixtures shall be avoided, particularly during ramp-up and ramp-down.

4.1 **Ramp-up**

4.1.1 The time to reach stable temperature and relative humidity conditions shall be less than 3 hours.

4.1.2 Condensation shall be avoided by ensuring that the test chamber (dry bulb) temperature exceeds the wet-bulb temperature at all times, and that the rate of ramp up shall not be faster than a rate which ensures that the temperature of any DUT does not lag below the wet bulb temperature.

4.1.3 The dry- and wet-bulb temperature set points shall be maintained so that the relative humidity is not less than 50% after significant heating begins. In a dry laboratory, the chamber ambient may initially be drier than this.

4.2 **Ramp-down.**

4.2.1 The first part of ramp-down to a slightly positive gauge pressure (a wet bulb temperature of about 104°C) shall be long enough to avoid test artifacts due to rapid depressurization, but shall not exceed 3 hours.

4.2.2 The second part of ramp-down from a wet bulb temperature of 104°C to room temperature shall occur with the chamber vented. There is no time restriction, and forced cooling of the vessel is permitted.

4.2.3 Condensation on devices shall be avoided in both parts of the ramp down by ensuring that the test chamber (dry bulb) temperature exceeds the wet-bulb temperature at all times.

4.2.4 Ramp-down should maintain the moisture content of the molding compound encapsulating the die. Therefore, the relative humidity shall not be less than 50% during the first part of the ramp-down (Sec. 4.2.1).

4.3 **Test Clock.** The test clock starts when the temperature and relative humidity reach the set points, and stops at the beginning of ramp-down.

4.4 **Bias.** Bias application during ramp-up and ramp-down is optional. Bias should be verified after devices are loaded, prior to the start of the test clock. Bias should also be verified after the test clock stops, but before devices are removed from the chamber.

4.5 **Readout.** Electrical test shall be performed not later than 48 hours after the end of ramp-down. Note: For intermediate readouts, devices shall be returned to stress within 96 hours of the end of ramp-down. The rate of moisture loss from devices after removal from the chamber can be reduced by placing the devices in sealed moisture barrier bags (without dessicant). When devices are placed in sealed bags, the "test window clock" runs at 1/3 of the rate of devices exposed to the laboratory ambient. Thus the test window can be extended to as much as 144 hours, and the time to return to stress to as much as 288 hours by enclosing the devices in moisture-proof bags.

4.6 **Handling.** Suitable hand-covering shall be used to handle devices, boards and fixtures. Contamination control is important in any highly-accelerated moisture stress test.

5.0 FAILURE CRITERIA

A device will be considered to have failed the Highly- Accelerated Temperature and Humidity Stress Test if parametric limits are exceeded, or if functionality cannot be demonstrated under nominal and worst-case conditions as specified in the applicable procurement document or data sheet.

6.0 SAFETY

Follow equipment manufacturer's recommendations and local safety regulations.

7.0 SUMMARY

The following details shall be specified in the applicable procurement document:

(a) Test condition letter.

(b) Test duration, if other than specified in 3.1.

(c) Measurements after test.

(d) Biasing configuration.

(e) Temperature of die during test if it is more than 5°C above the chamber ambient.

(f) Frequency and duty cycle of bias if cycled bias is to be used.