UNIVERSITY OF UTAH
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT

ANALOG INTEGRATED CIRCUITS LAB

LAB 5
Two-Stage CMOS Operational Amplifier and *C-V* Measurements

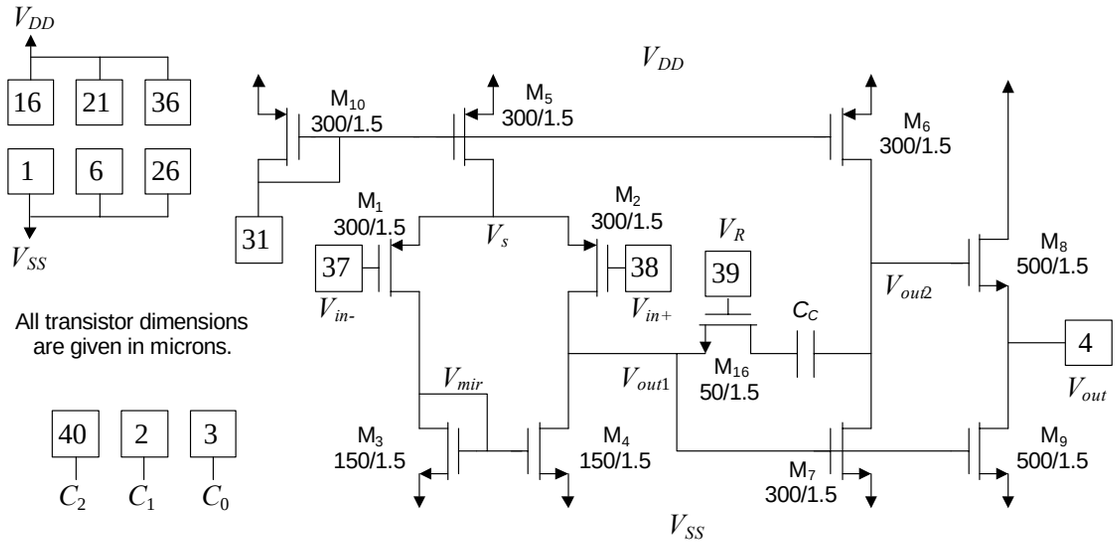
Objective: In this lab, you will characterize a two-stage CMOS operational amplifier. You should review sections 5.1-5.2 in Johns & Martin.

Power: This is the first lab where we will be using a *dual*-polarity power supply. This is also the first lab where we will use Chip B in addition to Chip A. We will use Chip B for Experiments 1 and 2. Connect pins 1, 6, and 26 of Chip B to V_{SS} = -2.5 V. Connect pins 16, 21, and 36 of Chip B to V_{DD} = +2.5 V. Note that this is equivalent to powering the chip from a single-polarity 5-V supply, but it allows us to reference signals around ground, which is conveniently located halfway between the two power supply rails. The substrate of this chip is now biased at -2.5 V. Leave these power connections in place for all experiments. Note that all voltages connected to the chip should be between -2.5 V and +2.5 V.

Experiment 1: Op-Amp Compensation

The following figure shows the subcircuits on Chip B that we will use for this characterization of the two-stage operational amplifier. **Be sure to connect pins 1, 6, and 26 to V_{SS} (-2.5 V), and pins 16, 21, and 36 to V_{DD} (+2.5 V) for all the experiments in this assignment.** Also, tie pins 8 and 9 to V_{SS}. This will be explained later in the lab.

Pin-out for Lab 5 – Chip B



Note that this amplifier is nearly equivalent to Fig. 5.2 (p. 222) in Johns & Martin. Of course, we are using a different process technology than the one presented in the book, so our numerical analysis of the circuit will differ. Also, since we are using an n-well process, we cannot connect the body of M_8 to its source (because the body of M_8 is the substrate), so the body effect will limit our output voltage swing a bit more.

The on-chip compensation capacitor C_C actually consists of three capacitors in parallel, with CMOS transmission gates (see Fig. 10.2 in Johns & Martin) to switch each capacitor in or out of the circuit. The binary signals C_0, C_1, and C_2 control these switches. The following table gives the equivalent value of C_C for each binary input:

C_2 (pin 40)	C_1 (pin 2)	C_0 (pin 3)	C_C
V_{SS}	V_{SS}	V_{SS}	–
V_{SS}	V_{SS}	V_{DD}	0.5 pF
V_{SS}	V_{DD}	V_{SS}	9.1 pF
V_{SS}	V_{DD}	V_{DD}	9.6 pF
V_{DD}	V_{SS}	V_{SS}	56.8 pF
V_{DD}	V_{SS}	V_{DD}	57.3 pF
V_{DD}	V_{DD}	V_{SS}	65.9 pF
V_{DD}	V_{DD}	V_{DD}	66.4 pF

(a) Pencil-and-paper analysis. Fill in the table below, using the following values, which represent average results from previous labs. Assume we bias the op-amp with 100 μA through M_{10}. Note that you can calculate all of these values using only the V_{t0} and $\mu C_{ox}'$ terms. (Calculate V_{eff} directly from I_D.)

<u>*n*MOS</u>
V_{t0} = 0.62 V
$\mu_n C_{ox}'$ = 40 μA/V^2
γ = 0.55 V$^{1/2}$
κ = 0.70
$V_A|_{L\,=\,1.5\,\mu m}$ = 50 V

<u>*p*MOS</u>
V_{t0} = -0.90 V
$\mu_p C_{ox}'$ = 20 μA/V^2
γ = 0.60 V$^{1/2}$
κ = 0.75
$V_A|_{L\,=\,1.5\,\mu m}$ = 50 V

device	I_D **(μA)**	g_m **(μA/V)**	r_{ds} **(kΩ)**	V_{eff} **(V)**
M_1				
M_2				
M_3				
M_4				
M_5				
M_6				
M_7				
M_8				
M_9				
M_{10}				

We define the following gains for the amplifier:

$$A_1 \equiv \frac{v_{out1}}{v_{in+} - v_{in-}}$$

$$A_2 \equiv \frac{v_{out2}}{v_{out1}}$$

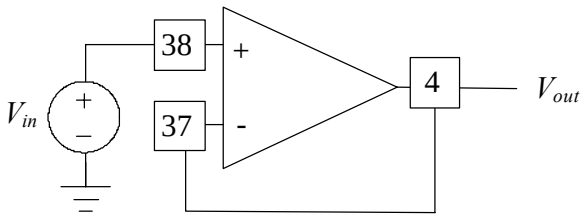
$$A_3 \equiv \frac{v_{out}}{v_{out2}}$$

$$A \equiv A_1 A_2 A_3 = \frac{v_{out}}{v_{in+} - v_{in-}}$$

- Write an analytical expression for each gain, and calculate its numerical value both in V/V and dB.

(b) Basic op-amp compensation. We will begin by biasing the op-amp so that the drain current of M_{10} is close to 100 μA. You will probably want to use a resistor from pin 31 to V_{SS} to set this bias current. Let's minimize the effect of M_{16} for now by tying pin 39 to V_{DD}. Set the compensation capacitor C_C its maximum value of 66.4 pF.

Configure the op-amp as a unity-gain follower, as shown below. Connect the function generator to the positive input. Observe the input on one channel of your oscilloscope and the output on the other channel. Make sure you tie the negative terminal of the function generator and oscilloscope probes to *ground*, not V_{SS}.



Apply a 1 kHz, 500 mVpp (peak-to-peak) square wave to the op-amp. (Remember to set the function generator to HIGH-Z mode!) Your op-amp should be acting as a unity-gain buffer. Observe both channels on the scope so you can compare input to output. Use the HP Benchlink Scope software on the PC to capture a screenshot of the scope.

- Include this screenshot in your report. Use this tool whenever you wish to include a scope screen in your report.

Now change the input to a 500 kHz, 200 mVpp square wave, and adjust the time scale and vertical gain on the scope so you have a clear view of the input and output waveforms. You should zoom in so you see about 1-2 complete cycles of the square wave on the screen. Set the scope to trigger on the input waveform.

- Can you see the bandwidth limitations of the op-amp? What do you think the phase margin of the op-amp is, based on its closed-loop response to a square wave? Use the figures handed out in class to estimate the phase margin of the op-amp with C_C = 66.4 pF to the nearest 5 or 10 degrees.
- Include a scope screen plot.

Now reduce C_C to 56.8 pF. Can you see a small change in the rise time or overshoot of the output?

- Again, estimate the phase margin and include a scope screen plot.

Now reduce C_C to 9.1 pF. Can you see a small change in the rise time or overshoot of the output? Do you see ringing? Estimate Q for this value of C_C.

- Use this value of Q to estimate the phase margin. Include a scope screen plot.

- Now reduce C_C to 0.5 pF. What happens to the output? Is the op-amp stable? Include a scope screen plot.

(c) Lead compensation. Now set C_C to 9.1 pF. Adjust V_R (pin 39) to add lead compensation to the circuit. It is recommended that you generate V_R using the +6V power supply with its negative terminal tied to V_{SS}. Now by adjusting the +6V supply between zero and 5.0 V, you can sweep V_R between V_{SS} and V_{DD}.

- How does V_R affect the compensation?
- Include a couple of relevant scope screen plots. What is the "best" value for V_R? (You may judge what "best" means in this case.)
- What is the value of $R_C = r_{ds16}$ (in triode region) in this case? (Note: You can use the value of V_{T0} and V_{eff7} to calculate V_{GS7}, which will give you the source voltage of M_{16}.) In Johns & Martin, p. 243, the authors recommend using a value of $R_C \cong 1/(1.2 \cdot g_{m1})$.
- How does your value of R_C compare with this recommended value? Set V_R to give this recommended value of R_C. (Remember to *measure* V_R with respect to ground, not V_{SS}.) Is the circuit compensated well?
- Include a scope screen plot.

Experiment 2: Op-Amp Performance

For the remainder of this lab, set C_C = 56.8 pF and $V_R = V_{DD}$. This seems to provide the best all-around compensation of this op-amp under our biasing conditions. We will now characterize the performance of this op-amp.

(a) Unity-gain frequency. We will now measure the unity-gain frequency f_t of the amplifier, which is equal to its gain-bandwidth product. Apply a 200 mVpp sine wave to the op-amp (configured as a unity-gain buffer) and increase the frequency of the sine wave until the gain of the amplifier drops from unity to approximately 0.707 (= -3 dB). This is the unity-gain frequency.

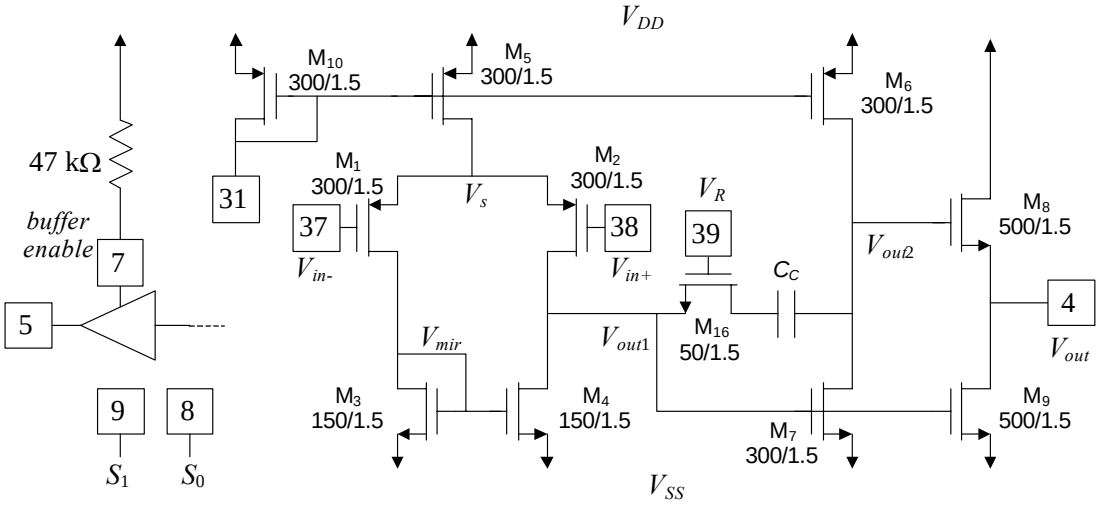
- How does your measured result agree with the theoretical prediction $f_t = g_{m1}/(2\pi C_C)$? Predict the closed-loop gain of a system using this op-amp and a feedback factor of $\beta = 0.001$.

(b) Slew rate. Apply a 100 kHz, 2 Vpp square wave to the unity-gain amplifier. Observe the input and output waveforms on the scope. Can you see the output slew? Adjust the frequency of the waveform if necessary. Using the cursors on the oscilloscope, measure the up-going and down-going slew rate of the op-amp, expressing the answer in V/μs.

- How do your measured results agree with the theoretical prediction of I_{D5}/C_C? Include a scope screen plot.
- Briefly change C_C to 9.1 pF and measure the slew rate. What happens? How does this compare with theory? Now return C_C to 56.8 pF.

(c) Offset voltage. Tie the input to ground and use a voltmeter to measure the output voltage. This is the input offset voltage.

(d) Internal nodes and gains. Our chip includes a unity-gain buffer that allows us observe four internal nodes of the op-amp without loading these internal nodes with the relatively large capacitance (several pF) of an op-amp probe. The figure below shows the buffer, whose output is on pin 5. To enable the buffer, tie a 47-kΩ resistor between pin 7 and V_{DD}. Pins 8 and 9 are digital control signals S_1 and S_0 that allow us to select which internal node voltage we wish to observe. The table below gives the voltages that appear on pin 5 for each select signal:



S_1 (pin 9)	S_0 (pin 8)	Output (pin 5)
V_{SS}	V_{SS}	V_s
V_{SS}	V_{DD}	V_{mir}
V_{DD}	V_{SS}	V_{out1}
V_{DD}	V_{DD}	V_{out2}

Now apply a 10 kHz, 5Vpp sine wave to the op-amp, which should still be configured as a unity-gain follower. First look at the output of the op-amp V_{out} (pin 4). What is $V_{out\ min}$ and $V_{out\ max}$? Now observe V_{out} and V_{out2} simultaneously.

- What is the value of V_{out2} when V_{out} hits its maximum value? Can you see a reason for the maximum output voltage? What is happening?

- Now observe the input voltage and V_s simultaneously. Based on these waveforms, can you suggest a minimum and maximum input voltage for the op-amp? You may also wish to look at V_{mir} and V_s simultaneously. What transistors are going out of saturation? Explain the input voltage limitations of the first stage.

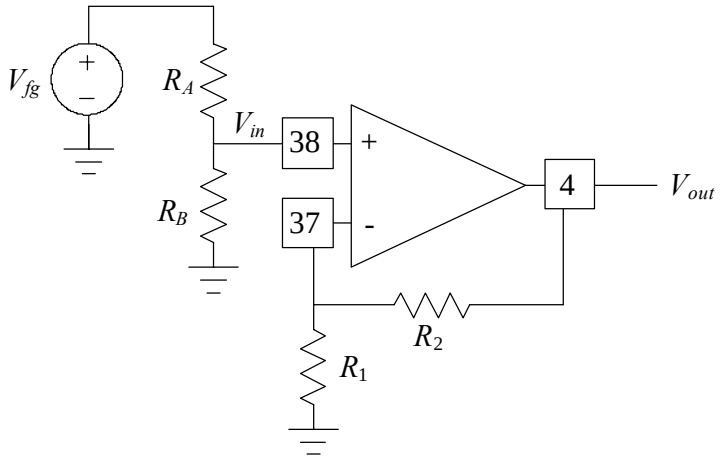
We will now measure the gain of each stage of the op-amp. Apply a 10 kHz, 1.5 Vpp sine wave to the op-amp.

- Observe the voltage amplitudes at V_{out} and V_{out2}, and use this to calculate A_3.
- Observe the voltage amplitudes at V_{out1} and V_{out2}, and use this to calculate A_2. (The voltage swing at V_{out1} will be *very* small; do the best you can to estimate its amplitude using the cursors on your scope.) How do these values compare to your calculated values?

Now we need to measure A_1. In theory, we could measure the voltage difference across the inputs V_{in+} and V_{in-} and compare this with the amplitude of V_{out1}, but this voltage is much too small for us to measure. We will measure A_1 by first measuring the gain of the entire op-amp A using an indirect method outlined below.

Configure the op-amp as a non-inverting amplifier, as shown below. Use the following resistor values: R_1 = 1 kΩ, R_2 = 1 MΩ, R_A = 100 kΩ, R_B = 1 kΩ. Measure the exact resistance of each resistor before adding it to the circuit, and use these exact values in all your calculations for maximum precision.

- Calculate the feedback factor β for this circuit. What would the closed-loop gain be if A were infinite?



We are using the resistor divider R_A-R_B to attenuate the waveform from the function generator. Set the function generator to provide a 100mVpp sine wave.

- Based on your measured values of R_A and R_B, calculate the expected signal level at V_{in}. Now measure the peak-to-peak amplitude of V_{out}. One problem with high-gain amplifiers such as this one is that in addition to amplifying the signal, they also amplify the op-amp offset voltage. You will need to adjust the offset voltage on your function generator to compensate for this affect. (Try to make the dc level of V_{out} equal zero.)
- Now adjust the frequency of the input signal and measure the 3-dB bandwidth of this amplifier. (It will be quite low!) Does this match your calculations based on f_t?

Now use an input sine wave at least a factor of 10 below the amplifier bandwidth so we get a reliable low-frequency gain measurement.

- What is the closed-loop gain $A_f = V_{out}/V_{in}$? Now use your calculated value of β to calculate A.
- From this, you can calculate A_1. Compare the measured values of A_1, A_2, A_3, and A to your calculated values.

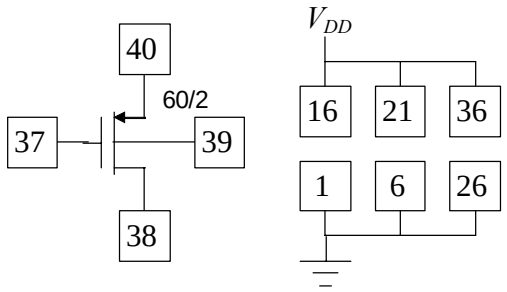
Experiment 3: *C-V* Measurement of a *p*MOS Capacitor

Experiment 1 demonstrated that moderate-sized integrated capacitors are often needed to compensate op-amps. On our lab chips, the capacitor C_C is built as a poly-poly2 capacitor. In many "digital" VLSI processes (which analog designers often find themselves using), a second poly layer is not provided. Metal-to-poly and metal-to-metal capacitances are typically kept low to minimize crosstalk, so the only way to build capacitors on the order of picofarads is to use the gate capacitance of a MOSFET. We will now take a short side trip to investigate the behavior of these "MOScaps".

In this experiment you will use the Keithley 590 CV meter in conjunction with the Keithley 4200 Semiconductor Characterization System (SCS) unit to take two capacitance-versus-voltage curves of a *p*MOS transistor configured as a capacitor. You will observe how the capacitance changes as the transistor moves from strong inversion ($V_{GS} < V_T$ for pMOS) to weak inversion ($V_T > V_{GS} > 0$ for pMOS) to accumulation ($V_{GS} > 0$ for pMOS).

Pin-out for Experiment 3 – Chip A

All transistor dimensions are given in microns.



Note that we are using Chip A for this experiment!

Power: You will need to use the Agilent E3631A power supplies that are located near the 4200s. Because of the way in which the 590s sweep the voltage, you will need a dual power supply. Use the +20V, -20V, and COM connections on the power supply. Connect pins 16, 21, and 36 to the +20V connection and set Vdd = 2.5 V. Pins 1, 6, and 26 are connected to the -20V connection which is set to Vss = -2.5 V. The common connection is the GND connection, and this is connected to the ground terminal on the 590 CV meter (more on this later). These connections are necessary to power the protection circuitry that is present on the chip. Failure to make these connections will result in faulty measurements taken by the 590.

Procedure: Before you begin make sure that the machines are powered on. The power switch is located on the front in the lower right. Before turning on the Keithley 4200, you must turn on the Keithley 590 CV meter first, or the 4200 will not boot up properly. To log on to the Keithley 4200, wait for the login prompt and enter:

Username: kiuser
Password:

Note that there is no password; just enter the username and hit enter. Once you are logged in to the machine the Keithley Interactive Test Environment (KITE) should automatically start up. If it does not, simply click on the icon labeled KITE.

Verify that the open project is the "pMOS_Capacitor" project. It will say this in the 'project view' in the window on the left side of the screen. If this is not the open project, click on File -> Open project and open the project file in C:S4200\kiuser\projects\pMOS_Capacitor\

Once you open the project, save a copy in a different folder, and use your new copy of the project to avoid making changes to the original.

Once the project is open you should see a list of parameters in the main window. If you do not see this then double click on the user test module (UTM) at the bottom of the project tree or click on the definitions tab at the top of the main window. The project tree is located in the left-most window.

Now you need to configure the 590. In the main window there is a list of parameters and below that there is a help box. The help box begins with telling you what kind of test module you are running. In this case it should say 'Module: CVSweep 590.' The CVSweep tells you that the device will sweep a voltage and measuring the capacitance, and the 590 tell you what test equipment the 4200 is trying to use. The help window is very useful in that every input that can be changed in the main window will have an entry and explanation in the help window. If, at any time you want to check the valid inputs for an entry, or what to see what the entry controls just check in the help window.

Begin by setting the following parameters:

Parameter	Setting	Function
Offset Correct	0	
Waveform	1	Sets a Single staircase sweep
First Bias	-2.4	Sets the start voltage of the sweep
Last Bias	2.4	Sets the stop voltage of the sweep
Step	0.05	Step size of the sweep
Frequency	0	Selects a test signal of 100 kHz

Default Bias	0	Sets the bias applied before and after the test
Start Time	Default	Time from when the test is started to when the first measurement is taken
Step Time	Default	Time in between steps
Range	2	Sets the larges measurable capacitance and effects the resolution
Model	0	Selects parallel model
Filter	1	Enables the analog filter
Reading Rate	3	Sets the rate at which the 590 takes its readings

See the help window for a further explanation of the parameters listed above. These are the parameters that will be used for both measurements. Once everything is properly set up, click on the "save" button at the top of the screen.

For the first measurement connect the source, drain, and body connections together. That is, connect pins 38, 39, and 40 together. This will serve as one terminal of the *p*MOS capacitor. The other terminal will be the gate: pin 37. You must connect the device to the CV meter. There are two connections on the CV meter: one labeled input and the other labeled output. During the voltage sweeps the 'input' terminal is held at a constant voltage while the 'output' terminal is swept. Connect the 'input' to the body-source-drain terminal of the capacitor. Connect the 'output' to the gate terminal of the capacitor. Also connect the ground terminal of the input to the COM terminal of the power supply. This ensures that the CV meter is using the same GND reference as the chip.

Once everything is connected properly and the power supply is turned on, click the green play button at the top of the screen. This will begin the test. You can click the red stop button at any time to stop the currently running measurement. You can tell when the 590 is finished taking the measurement when the red stop button is grayed out, or when the status window at the bottom reads:

"Stop execution…
Total Execution time…"

You will see the CV meter begin sweeping the voltage while measuring the capacitance. The far right display on the CV meter is the current voltage being applied to the capacitor while the left display give the measured capacitance and conductance. If you see the word OVERLOAD appear on the CV meter, your range is set too low; simply increase the range setting.

To view a plot of the data just measured, click on the graph tab at the top of the main window. Now right click anywhere in the graph and select "Define Graph." You should see a window with all of the data measured down one side and the X, Y1, and Y2 axis along the top. Click the box at the intersection of V and X. This sets the X axis to be the swept voltage. Now set the Y1 axis to C. Click OK.

Right click on the graph once again and select auto scale. You should now see a plot of the capacitance versus the voltage. The X axis is actually V_G-V_S. So the right hand side of the plot shows the transistor is in accumulation while the left side corresponds to strong inversion. You should see high capacitance (C_{ox}) for the accumulation and strong inversion regions. In accumulation, the n^- channel is converted to n^+ because additional electrons are attracted by the positive charges on the gate. They *accumulate* at the surface of the channel and provide a highly-conductive "bottom plate" for the capacitor. In strong inversion, the channel is inverted to p^+, and the p^+ source provides an unlimited supply of holes to the channel. In weak inversion, the channel is not electrically connected to the source, so the overall capacitance is the series combination of the oxide capacitance C_{ox} and the depletion capacitance C_{dep} between the p^- channel (weakly inverted) and the n^- well. Capacitance in weak inversion is usually one-half to one-third of C_{ox}.

It is important to note here that the capacitance measured includes the parasitic capacitance of the breadboard, the capacitance from one pin to another in the package, capacitance from one bond wire to another, etc. In order for the actual capacitance of the *p*MOS capacitor to be seen all of these parasitic capacitances must be subtracted out. These parasitic capacitances have been measured to be around 4 pF, but the exact number may vary from one breadboard to the next. To correct for this, use the known maximum value (e.g., in accumulation) of this MOS capacitor: 0.3 pF. In MATLAB, subtract the necessary value to make your maximum capacitance equal this value. Report the value you subtracted in your report.

In order to save your data for later use in MATLAB, click the "sheet" tab at the top of the main window. This shows all of the data values taken by the 4200 when running the measurement. Insert a 3.5 inch floppy drive into the disk drive and click on the "save as…" button. You can save your data in .xls, .txt, or .csv format.

For the second measurement simply disconnect pins 38 and 40, the source and drain, and leave them floating. Now the CV meter should only be connected to the gate of the transistor and the body of the transistor. Run the test again.

This time you should see the capacitance at a maximum in accumulation and then at a minimum when the transistor is in strong inversion. In this case, the p^+ source and drain can no longer provide a reservoir of holes to the channel. Since the channel is doped n^-, the only source of holes is through thermal generation. Thermal generation cannot work fast enough to provide the needed holes at high frequencies, and the capacitance stays low.

- In your report, provide *C-V* plots for both cases, and label the different regions of operation.

EXTRA CREDIT (5 points)

We are operating the op-amp transistors at fairly low current levels near the edge of strong and moderate inversion. In this region, the traditional above-threshold expression for g_m overestimates transconductance. A better expression that works over *all* operation regions (weak, moderate, and strong inversion) is given by the EKV model:

$$g_m = \frac{\kappa I_D}{U_T} \cdot \frac{2}{1+\sqrt{1+4 \cdot \mathrm{IC}}}$$

where U_T is the thermal voltage kT/q and IC is the inversion coefficient of the transistor:

$$\mathrm{IC} = \frac{I_D}{I_S}$$

where, I_S is the *moderate inversion characteristic current*, given by

$$I_S = \frac{2\mu C'_{ox} U_T^2}{\kappa} \cdot \frac{W}{L}$$

An inversion coefficient of 10 or greater indicates the transistor is operating in strong inversion and traditional above-threshold equations may be used. An inversion coefficient less than 0.1 indicates the transistor is operating in weak inversion, and the subthreshold equations may be used. Values of IC between 0.1 and 10 indicate moderate inversion operation, where the EKV model should be used.

Calculate the inversion coefficient for M_1-M_{10}, and recalculate the transconductance of each devices using the EKV model. Re-work *all* theoretical calculations in this lab that make use of g_m, and comment on how the revised calculations compare to your experimental measurements. Does theory match experiment better with this model?

REPORT

Each lab group (two students) should submit a lab report that is separate from the lab notebook. (In this class, lab notebooks will not be turned in). The report should be typed, not handwritten, although it is acceptable to add neat handwritten notes to figures where appropriate (e.g., to label different curves). Lab reports are due in your lab section one week after a two-week lab ends.

Begin your lab report with a title page containing your names, email addresses, T.A., lab section, and the title of the lab. Next, write one or two paragraphs outlining the overall goal of the lab. Describe how you performed each experiment, listing any problems you encountered and how you overcame them. Figures are preferably included in line with the text. You should number the figures and refer to them from the text.

- Every sentence labeled with a "bullet" like this indicates either a figure you should include or an answer you should explicitly provide in your report.

The grading for lab 5 will be as follows:

Screenshots, Plots (9):	4 points each
Answers (16):	2 points each
Tables (2):	5 points each
Introduction and conclusion:	4 points
Format and style:	3 points
Total:	85 points

Extra credit: 5 points

Your lab report should contain a description of all experiments performed, data plots (with fits) requested throughout this assignment, and a discussion of how the measured data (and fit parameters) compare with circuit theory. At the end of your lab report, create a "data sheet" for your op-amp as shown on the following page.

Op-Amp Data Sheet

parameter	**value**	**units**
Power supply current		mA
Power dissipation (no load) (V_{DD} = +2.5 V, V_{SS} = -2.5 V)		mW
unity-gain bandwidth f_t		MHz
low-frequency gain A		dB
slew rate (+)		V/μs
slew rate (-)		V/μs
input offset voltage		mV
V_{out} (max)		V
V_{out} (min)		V
V_{in} (max)		V
V_{in} (min)		V
phase margin		degrees